C. Remarks

This Response is a submission under 37 C.F.R. § 1.114 in connection with a Request for Continued Examination (RCE).

In the office action, claims 17, 98-101, 103, 125, 126, and 128 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Moravvej-Farshi *et al.* ("Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain," Solid State Electronics, Vol. 30, No. 10, 1987, pp. 1053-1062) ("Moravvej-Farshi") in view of Wolf *et al.* ("Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET," 1995, pp. 232-240 and 309-311) ("Wolf"). Claim 102 stands rejected under § 103(a) as being unpatentable over Moravvej-Farshi and Wolf in view of U.S. Patent No. 6,130,482 to Iio *et al.* ("Iio"). Applicants respectfully traverse the rejections as follows.

Section 103 Rejections

Claims 17, 98-103, 125, 126

Applicants have amended claim 17 to recite that the transistor formed on a substrate assembly includes:

> a raised drain structure;
>
> a raised source structure;
>
> a gate located between said source and said drain;
>
> a first capping layer in communication with at least a portion of said gate and said source;
>
> a first portion of a gate oxide region in communication with at least a portion of said gate and said source;
>
> a first pocket implant junction located in said substrate assembly, said first pocket implant junction comprising a first high dose dopant implant and defining a first low-resistance path, wherein said first pocket implant junction is in communication with said source ***predominantly along a non-sidewall portion thereof*** and extends under a first portion of said gate;

> a second capping layer in communication with at least a portion of said gate and said drain;
>
> a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and
>
> a second pocket implant junction located in said substrate assembly, said second pocket implant junction comprising a second high dose dopant implant and defining a second low-resistance path, wherein said second pocket implant junction is in communication with said drain ***predominantly along a non-sidewall portion thereof*** and extends under a second portion of said gate.

Applicants submit that support for this amendment may be found throughout the specification and figures as filed, such as, for example, in Figures 7-11.

Applicants submit that a *prima facie* case of obviousness under 35 U.S.C. §103(a) requires, among other things, that the cited references, when combined, teach or suggest every element of the claim. *See* MPEP §2142. Applicants submit that the Office has not established a *prima facie* case of obviousness because not all elements of claim 17 are taught or suggested by the cited references.

More specifically, Applicants submit that Moravvej-Farshi, Wolf, and Iio, either alone or in combination, fail to teach or suggest, among other things, a transistor formed on a substrate assembly that includes:

> a first pocket implant junction located in said substrate assembly, ... wherein said first pocket implant junction is in communication with said source predominantly along a non-sidewall portion thereof ...; [and]
>
> a second pocket implant junction located in said substrate assembly, ... wherein said second pocket implant junction is in communication with said drain predominantly along a non-sidewall portion thereof ...,

as recited in claim 17.

Applicants submit that Moravvej-Farshi discloses a technique for self-aligning a polysilicon gate in devices having polysilicon source and drain regions. *See, e.g.*, Abstract. As conceded by the Examiner at pages 2-3 of the office action, neither this technique nor device structures fabricated thereby teach or suggest "a first pocket implant junction" and "a second pocket implant junction," as recited in claim 17.

Applicants submit that Wolf discloses at pages 235-40 several techniques for preventing subsurface punchthrough in short-channel MOSFETs. A first technique includes implanting p-type dopants under the lightly-doped tip region of the lightly-doped drain (LDD). *See* page 238, page 240, Figure 5-25(a). Wolf discloses that a dopant implant formed according to this technique "raises the doping concentration only on the inside walls of the source/drain junctions," thus permitting the channel length to be decreased without the use of a higher-dosed substrate. *See* page 238. Because the first and second pocket implant junctions of claim 17 are in communication with the source and drain "predominantly along a non-sidewall portion thereof," respectively, each is clearly distinguished from the dopant implant formed using the first technique disclosed by Wolf.

Citing the teachings of A. Hori *et al.* ("A Self-Aligned Pocket Implantation (SPI) Technology for 0.2 um-Dual Gate CMOS," Tech. Dig. IEDM, p. 641,1991) ("Hori I"), Wolf discloses a second technique for preventing subsurface punchthrough wherein a halo-like device, or "self-aligned pocket implantation," is formed using large-angle tilt (LAT) implantation of boron ions in NMOS and phosphorous ions in PMOS. See page 238, page 240, Figure 5-25(c). Regarding the features of Figure 5-25(c), the Examiner states: "[T]he p+ pocket implants extend a short distance under the source and the

drain, this short distance is the area where the pocket implant junctions are in communication with a non-sidewall portion of the source and drain." Without acquiescing to the Examiner's assertion that Moravvej-Farshi and Hori I (as cited by Wolf) are properly combinable, Applicants respectfully disagree with the Examiner regarding any extension of the p+ pocket implants under the source and drain depicted in Figure 5-25(c). The extensions cited by the Examiner are not readily apparent on the p+ pocket implants of Figure 5-25(c) as drawn, and the presence of titanium silicide layers masking virtually all of the source and drain regions suggests that extension formation under the source and drain is not physically possible.

In particular, the masking effect of the titanium silicide layers used in the second technique disclosed by Wolf is more fully discussed in U.S. Patent No. 5,320,974 to Hori et al. ("Hori II") in connection with Figure 12(c) therein (reproduced below). A copy of the Hori II reference is submitted herewith. With respect to the process depicted by

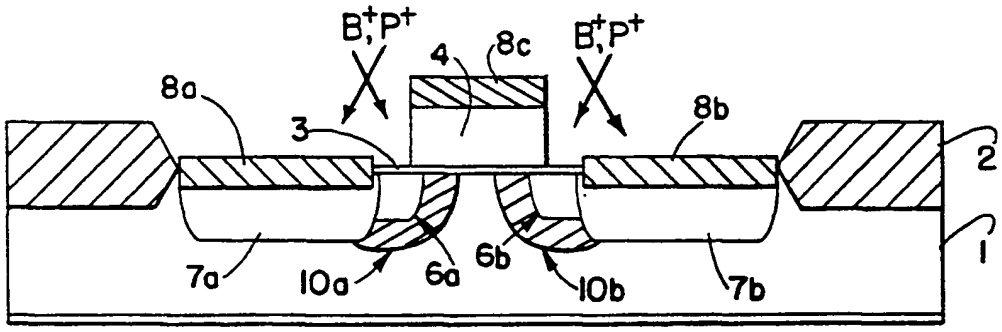


FIG. 12C

Figure 12(c), it is stated at column 11, lines 55-61 that "[s]ince an stopping power of titanium silicide is about 1.5 times higher than that of silicon, ***boron ions are not allowed to permeate near pn-junctions between the n+-type source and drain regions 7a and 7b and the substrate1. Therefore, it is easy to form the p+***

semiconductor regions only in the channel region." (emphasis added). Applicants note that process steps of Figure 12(c) and the features formed thereby are identical in all key respects to those in the bottommost diagram of Figure 5-25(c) of Wolf cited by the Examiner. Moreover, Applicants note that Figure 12(c) of Hori II is an intermediate processing step and that the transistor device of Figure 12(d) (reproduced below) created by applying subsequent processing steps to the device of Figure 12(c) clearly shows the absence of any extensions under the source and drain.

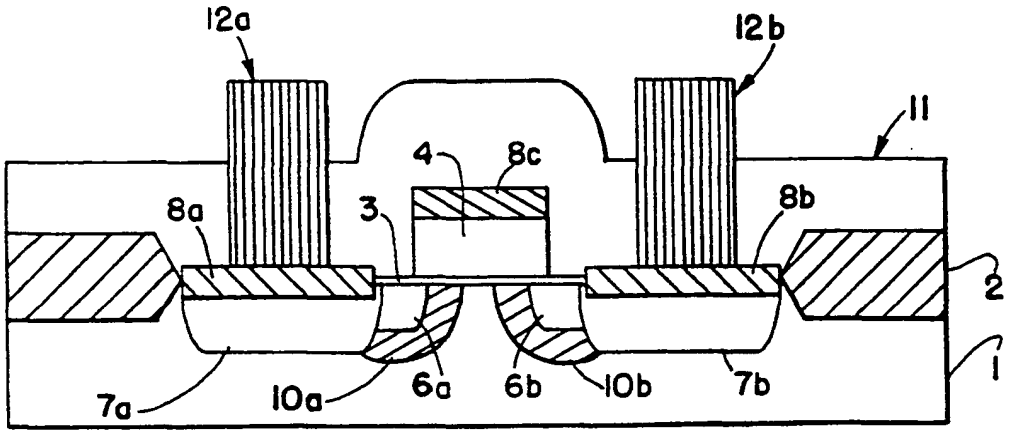


FIG. 12D

Notwithstanding the teachings of Hori II that the titanium silicide layers in Figure 5-25(c) of Wolf likely preclude the implanted regions from extending under (*i.e.*, along non-sidewall portions of) the source or drain, Applicants submit that neither Wolf or any of the other cited references, alone or in combination, teach or suggest first and second pocket implant junctions wherein "said first pocket implant junction is in communication with said source ***predominantly along a non-sidewall portion thereof***," and wherein "said second pocket implant junction is in communication with said drain ***predominantly along a non-sidewall portion thereof***," as recited in claim 17. To the contrary, Applicants submit that the implanted regions of Figure 5-25(c) of Wolf are

predominantly (if not entirely) in communication with sidewall portions of the source and drain.

For at least the above reasons, Applicants submit that claim 17, as well as claims 98-103 depending therefrom, are nonobvious over the cited references, either alone or in combination. *See* MPEP §2143.03 (stating that if an independent claim is nonobvious under §103(a), then any claim depending therefrom is nonobvious). Accordingly, Applicants respectfully request that the §103 (a) rejections of claims 17 and 98-103 be withdrawn.

Claims 125-126

Claim 125 is directed to a transistor formed on a substrate assembly and has been amended in a manner similar to claim 17. Therefore, for reasons analogous to those presented above with respect to claim 17, Applicants submit that claim 125, as well as claim 126 depending therefrom, are nonobvious over the cited references. Applicants therefore respectfully request that the § 103(a) rejection of claims 125-126 be withdrawn.

Claim 128

Claim 128 is directed to a transistor formed on a substrate assembly and has been amended to include:

> a halo implant structure located in said substrate assembly, said structure comprising a first pocket implant junction and a second pocket implant junction, wherein said first pocket implant junction includes a first high dose dopant implant in communication with said source predominantly along a non-sidewall portion thereof and extends under a first edge of said gate, and wherein said second pocket implant junction includes a second high dose dopant implant in communication with said drain predominantly along a non-

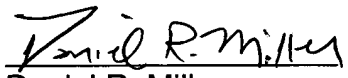
sidewall portion thereof and extends under a second edge of said gate.

Applicants submit that support for this amendment may be found throughout the specification and figures as filed, such as, for example, in Figures 7-11. For reasons analogous to those presented above with respect to claim 17, Applicants submit that claim 128 is nonobvious over the cited references. Applicants therefore respectfully request that the § 103(a) rejection of claim 128 be withdrawn.

D. Conclusion

Applicants respectfully request issuance of a Notice of Allowance for the subject application. If the Examiner is of the opinion that the subject application is in condition for disposition other than allowance, the Examiner is respectfully requested to contact the undersigned representative at the telephone number listed below, in order that the Examiner's concerns may be expeditiously addressed.

Respectfully submitted,



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